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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,484	08/10/2000	Walter David Braddock IV	OSEM-DB3	6691

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EXAMINER	
KANG, DONGHEE	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/636,484	BRADDOCK, WALTER DAVID	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 21 & 26, 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 36-142* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-26,37,39-55,57-59,64-89,91,93-109,111-113,118-122,125-134,136-138,141 and 142* is/are allowed.

6)☒ Claim(s) *36,38,56,60-63,90,92,110,114-117,123,124,135,139 and 140* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/27/02, 4/14/02 & 8/24/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. In view of the reply brief filed on 07/26/04, PROSECUTION IS HEREBY REOPENED. Rebuttal to the reply brief is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Furthermore, any submission of the claim must be consistent with the amendment filed 4/29/03 pursuant to the petition decision.

Information Disclosure Statement

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field 2/27/2002, 4/14/2002 and 8/24/2004.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 123-124, 135, & 139-140 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claims 123 & 139, the phrase "the GaAs-based supporting semiconductor structure is an at least partially completed heterojunction **bipolar transistor**" is not supported by the specification. The specification only discloses a MOSFET.

Re claim 124 & 140, the phrase "the GaAs-based supporting semiconductor structure is an at least partially completed **semiconductor laser**" is not supported by the specification. The specification only discloses a MOSFET.

Re claims 135, the phrase "the step of **evaporating Gd** commences before the step of evaporating atomic oxygen" is not supported by the specification.

Response to Amendment & Argument

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 60-63 & 114-117 are rejected under 35 U.S.C. 102(b) as being anticipated by Passlack (US 5,665,658).

Re claims 60 & 114, Passlack teaches a metal-oxide-compound semiconductor field effect transistor structure, comprising (Fig.3):

a compound semiconductor wafer structure (31, GaAs) having an upper surface; a gate insulator structure (35) comprising a first layer (35a, Ga_2O_3) and a second layer (35b, SiN: Col.2, lines 13-14), said gate insulator on said upper surface; said first layer substantially comprising compounds of gallium and oxygen; said second layer having a composition different than said first layer and a gate electrode (36) on said gate insulator structure. See also Col.4, lines 54-67.

Re claims 61 & 115, Passlack teaches a method for forming a metal-oxide-compound semiconductor field effect transistor structure, comprising (Fig.3):

Providing a compound semiconductor wafer structure (31, GaAs) having an upper surface; depositing a gate insulator structure (35) comprising depositing a first layer (35a, Ga_2O_3) and depositing a second layer (35b, SiN: Col.2, lines 13-14), said gate insulator on said upper surface; said first layer substantially comprising compounds of gallium and oxygen; said second layer having a composition different than said first layer and a gate electrode (36) on said gate insulator structure. See also Col.4, lines 54-67.

Re claims 62-63 & 116-117, Passlack does not explicitly teach said transistor has a quiescent state leakage current of less than many microamps. However, this feature is inherent in Passlack's device because the claimed and Passlack's product are identical in structure. See M.P.E.P 2112.01.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 36, 56, 90, & 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Passlack et al. (US 5,945,718) in view of Kikkawa (US 6,121,153).

Re claims 36 & 90, Passlack et al. teach an enhancement mode metal-oxide compound semiconductor field transistor (MOSFET) comprising (Fig.1):

a compound semiconductor wafer structure (12) having an upper surface; a gate oxide layer (14) positioned on upper surface of said compound semiconductor wafer structure; a gate electrode (17) positioned on upper surface of said gate oxide layer; source (21) and drain (22) ion implants self-aligned to the gate electrode; and source and drain ohmic contacts (19 & 20) positioned on ion implanted source and drain areas, wherein said compound semiconductor wafer structure comprises an InGaAs (24), AlGaAs (23) and GaAs (15) layers, said GaAs layer (15) is in contact with said gate oxide layer 14; and a GaAs substrate (11) on which resides said compound semiconductor wafer structure. See also Col.2, line 65 – Col.4, line 4.

The term "gate oxide layer" would meet the claimed term "gate insulator structure" because both terms functions insulating gate electrode from a semiconductor

layer in MOSFET device and the terms, gate oxide layer and gate insulator structure, are often used interchangeably in the art.

Passlack et al. do not teach an InP substrate. However, Kikkawa teaches that one may use InP for the substrate in place of GaAs (Col.16, lines 5-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute GaAs substrate of Passlack with InP substrate as taught by Kikkawa, since GaAs and InP are art recognized substrate for growing InGaAs compound crystal for semiconductor devices.

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) (Claims to a printing ink comprising a solvent having the vapor pressure characteristics of butyl carbitol so that the ink would not dry at room temperature but would dry quickly upon heating were held invalid over a reference teaching a printing ink made with a different solvent that was nonvolatile at room temperature but highly volatile when heated in view of an article which taught the desired boiling point and vapor pressure characteristics of a solvent for printing inks and a catalog teaching the boiling point and vapor pressure characteristics of butyl carbitol. "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301.). See MPEP 2144.07.

Therefore, it would have been obvious to one of ordinary skill in the art substitute InP for GaAs.

Re claims 56 & 110, Passlack et al. teach an upper spacer layer comprises $In_zGa_{1-z}P$ (See claim 13). Composition z of In can be interpreted between 0 and 1 because the composition y of In is not given in the specification and/or claim. If z composition of In is one, this compound becomes InP. Therefore, the $In_zGa_{1-z}P$ of Passlack would meet the claimed InP.

9. Claim 38 & 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Passlack et al. (US 5,945,718).

Passlack teaches an enhancement mode metal-oxide compound semiconductor field effect transistor comprising (Fig.1):

a compound semiconductor wafer structure (12) having an upper surface; a gate oxide layer (14) positioned on said upper surface; a gate electrode (17) positioned on upper surface of said gate oxide layer; source (21) and drain (22) ion implants self-aligned to the gate electrode; and source and drain ohmic contacts (19 & 20) positioned on ion implanted source and drain areas, wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer (23) and a narrower band gap channel layer (InGaAs, 24). See also Col.2, line 65 – Col.4, line 4.

Passlack in Fig.1 does not show that transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit. However, Passlack noted that complementary GaAs devices exhibit optimum speed/power performance and efficiency at a low supply

voltage of 1 V and below (Col.1, lines 18-24). This advantageous of complementary metal oxide semiconductor devices are well known in the art.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate transistor together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuit because of the well known advantages of CMOS configurations.

Allowable Subject Matter

10. Claims 1-26, 37, 39-55, 57-59, 64-89, 91, 93-109, 111-113, 118-122, 125-134, 136-138, & 141-142 are allowed.

Response to Arguments

11. Applicant's arguments filed July 26, 2004 have been fully considered but they are not persuasive.

Applicant argues that Ga2O3 is not insulating material and that the Passlack '718 patent's Ga2O3 layer is therefore not "a gate insulator". This assertion is supported by evidence of record, attachment 1 filed April 29, 2003.

This is not convincing.

Passlack et al. clearly teach that Ga2O3 is a gate oxide layer for metal-oxide-semiconductor FET (MOSFET), wherein the gate oxide layer functions to insulate the gate electrode from a semiconductor layer in order to properly operate the MOS FET device as disclosed by Passlack. If the Ga2O3 is not an insulator as asserted by

applicant, the MOS FET of Passlack is inoperative. **Every patent is presumed valid and the presumption includes the presumption of operability**. See M.P.E.P. 716.07. Therefore, it is clear that the Ga2O3 gate oxide layer must function as an insulator in order to operate as a MOSFET device as disclosed by Passlack.

The DECLARATION, filed July 21, 2004 is insufficient to overcome the rejection of claims 36 & 38 based upon Passlack et al. (US 5,945,718) as set forth in the last Office Action because of following reason:

The Declaration explains that Passlack patent (US 5,945,718) does not disclose a MOSFET because the Passlack' Ga2O3 layer as disclosed in the '718 patent does not provide the function of a gate insulator of a MOSFET.

First, through out at the disclosure of Passlack et al., the Ga2O3 is referred to as "a gate oxide layer". This phrase is understood in the art to mean an insulating layer.

Secondly, and more importantly, if the Ga2O3 layer is not an insulator, the device disclosed by Passlack et al. would be inoperative. MPEP 716.07 states "every patent is presumed valid, and the presumption includes the presumption of operability." Therefore, the statement presented in the Declaration misrepresents the invention of Passlack et al., and contradicts the fully operable device with Ga2O3 being an insulator.

Applicant argues that the $In_yGa_{1-y}As$ is not in contact with the gate insulator structure. This is not convincing. Value y of In can be interpreted between 0 and 1 because the composition y of In is not given in the specification or the claim. If y

composition is zero, this compound becomes GaAs. Passlack et al. clearly teach GaAs top layer 15 being in contact with gate insulator structure 14 (see figure 1).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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